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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,969	09/22/2003	Katsumi Abe	q75817	4962

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EXAMINER	
PHAM, TAMMY T	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
05/17/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/664,969	ABE, KATSUMI	
	Examiner	Art Unit	
	TAMMY PHAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 29-36* is/are pending in the application.

4a) Of the above claim(s) *8-15 and 22-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,16-21 and 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23 November 2009 has been entered.

Response to Amendment

2. Claims 27-28 have been cancelled. Claims 8-15, 22-26 have been withdrawn. Claims 1-7, 16-21, 29-36 are considered below.

Response to Arguments

3. Applicant's arguments filed 19 March 2010 have been fully considered but they are moot in view of the new grounds of rejection.

4. This application contains claims 8-15, 22-26 drawn to an invention nonelected. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-4, 17-19, 21, 29-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (U.S. Patent No.: 7,002,541 B2) in view of Okajima (U.S. Patent No.: 5,793,680) and Yatabe et al. (Japanese Publication No.: 2001-051662 as translated by U.S. Patent No.: 6,633,287 B1).

6. **In regards to independent claims 1, 33-34,** Yanagi teaches of a common drive circuit (Fig. 1, items 4-6) for a display (Fig. 1, item 12), the common drive circuit (Fig. 1, items 4-6) comprising:

7. a first voltage supply (Fig. 1, item Vcom2) and a second voltage supply (Fig. 1, item Vcom1) which respectively supply a high level voltage signal (Fig. 2, item Vcom2) and a low level voltage signal (Fig. 2, item Vcom1) to a common electrode (Fig. 1, item Vcom);

8. at least one signal line (Fig. 1, item Vref); and

9. at least one capacitance load (Fig. 1, items 4, 13) directly connected to respective terminals of the switch (Fig. 1, item 5c) not connected to the first and second voltage supplies (Fig. 1, items Vcom1, Vcom2),

10. wherein a high level of a signal passing through the at least one signal line (Fig. 1, item Vref1) is substantially equal to the high level voltage signal supplied by the first voltage supply (Fig. 1, item Vcom2) and a low level of the signal passing through the signal line (Fig. 1, item

Vref2) is substantially equal than the low level voltage signal supplied by the second voltage supply (Fig. 1, item Vcom1).

11. Yanagi fails to teach of at least one first transistor including either a drain or a source terminal connected to the first supply;

12. at least one second transistor including either a drain or source terminal connected to the second supply;

13. at least one signal line connected to each gate terminal of the first and second transistors; which controls the switching of the first and second transistors; and

14. at least one load connected to respective terminals of the first and the second transistors,

15. wherein a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by the first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by the second voltage supply.

16. Yatabe teaches of the concept of having a high level of a signal passing through the at least one signal line (Fig. 5, item VSP) is higher than the high level voltage signal supplied by the first voltage supply (Fig. 5, item VHP) and a low level of the signal passing through the signal line (Fig. 5, item Vcc) is lower than the low level voltage signal supplied by the second voltage supply (Fig. 5, item GND).

17. It would have been obvious to one with ordinary skill in the art at the time the invention was made to incorporate the concept of having higher and lower voltages of Yatabe and the display device of Yanagi. One of the benefits of this combination is that it helps cut cost by providing a more simplified circuit (Yatabe, column 1, lines 55-60).

18. Okajima teaches of at least one first transistor (Fig. 14, items 62, 66) including either a drain or a source terminal connected to the first supply (Fig. 14, item 15B);

19. at least one second transistor (Fig. 14, item 65, 69) including either a drain or source terminal connected to the second supply (Fig. 14, item 15B);

20. at least one signal line (Fig. 14, item L1) connected to each gate terminal of the first and second transistors (Fig. 14, items 62, 66 and 65 and 69) which controls the switching of the first and second transistors (Fig. 14, items 62, 66 and 65 and 69); and

21. at least one load (Fig. 14, item /CLKO) connected to respective terminals of the first and the second transistors (Fig. 14, items 62, 66 and 65, 69).

22. It would have been obvious to one with ordinary skill in the art at the time the invention was made to replace the switch of Yanagi with the first and second transistors as taught by Okajima as modified by the varying voltages of Yatabe. This combination would allow for a circuit with high speed signal frequency (Okajima, column 1, lines 8-10).

23. **In regards to independent claim 17,** in addition to the claim limitations of claim 1 above, Yanagi further teaches of a display (Fig. 1) comprising:

24. a substrate (Fig. 1):

25. a display portion (Fig. 1, item 13) integrated on the substrate; and

26. a gate driver circuit (Fig. 1, item 2) which controls switching of pixels (Fig. 1, item 13) of each line in a display portion (Fig. 1, item 13);

27. a common drive circuit (Fig. 1, items 4-6) for the display portion (Fig. 1, item 13) which simultaneously driving capacitance loads in the display portion (Fig. 1, item 13).

28. **In regards to claims 3, 18,** Yanagi as modified by Okajima and Yatabe above in claims 1, 17, teaches that at least one first transistor (Okajima, Fig. 14, items 62, 66) comprises P-type transistor (Okajima, Fig. 14, item 62) and the at least one second transistors (Okajima, Fig. 14, items 65, 69) comprises N-type transistor (Okajima, Fig. 14, item 69), and

29. wherein the gate terminals of the first (Okajima, Fig. 14, items 62, 66) and second transistors (Okajima, Fig. 14, item 62) are connected to common signal lines (Okajima, Fig. 14, item /CLKO).

30. **In regards to claim 4,** Yanagi as modified by Okajima, Yatabke, and Park above, teaches that the P-type transistors (Okajima, Fig. 14, item 62) and N-type transistors (Okajima, Fig. 14, item 66) are connected in parallel to be the first transistor (Okajima, Fig. 14, items 62, 66), and N-type transistors (Okajima, Fig. 14, item 69) and P-type transistors (Okajima, Fig. 14, item 65) are connected in parallel to be the second transistor (Okajima, Fig. 14, item 65, 69),

31. wherein respective gates of the P-type transistors of the first transistor (Okajima, Fig. 14, item 62) and the N-type transistor of the second transistors (Okajima, Fig. 14, item 69) are

connected to one the signal line (Okajima, Fig. 14, item L1), and respective gates of the N-type transistors of the first transistor (Okajima, Fig. 14, item 66) and the P-type transistors of the second transistor (Okajima, Fig. 14, item 65) are connected to an inversion signal line of one the signal line (Okajima, Fig. 14, item L2).

32. **In regards to claim 19,** Yanagi as modified by Okajima and Yatabe above in claims 1, 17, teaches that the P-type transistors (Okajima, Fig. 14, item 62) and N-type transistors (Okajima, Fig. 14, item 66) are connected in parallel to be the first transistor (Okajima, Fig. 14, items 62, 66), and N-type transistors (Okajima, Fig. 14, item 69) and P-type transistors (Okajima, Fig. 14, item 65) are connected in parallel to be the second transistor (Okajima, Fig. 14, item 65, 69),

33. wherein respective gates of the P-type transistors of the first transistor (Okajima, Fig. 14, item 62) and the N-type transistor of the second transistors (Okajima, Fig. 14, item 69) are connected to one the signal line (Okajima, Fig. 14, item L1), and respective gates of the N-type transistors of the first transistor (Okajima, Fig. 14, item 66) and the P-type transistors of the second transistor (Okajima, Fig. 14, item 65) are connected to an inversion signal line of one the signal line (Okajima, Fig. 14, item L2).

34. **In regards to claim 21,** Yanagi as modified by Okajima and Yatabe above in claims 1, 17, fails to teaches that the first and second transistors are comprised of thin-film transistors.

35. Examiner takes official notice that it is well known in the art to use thin-film transistors.

36. It would have been obvious to one with ordinary skill in the art at the time the invention was made to use thin-film transistors in the drive circuit of Yanagi as modified by Okajima, since the use of thin-film transistors enables a simple and cost efficient method to implement a switching method.

37. **In regards to claims 29, 31-32,** Yanagi as modified by Okajima and Yatabe above in claims 1, 17, teaches of a level shift circuit (Yanagi , Fig. 1, items 5a-b or Okajima, Fig. 14, item 60) connected to the one signal line directly (Yanagi , Fig. 1, item Vref1) {claim 29}; and

38. the inversion signal line directly (Okajima, Fig. 14, item 56) {claims 30-32}.

39. **In regards to claim 30,** Yanagi as modified by Okajima, Yatabke, Kubota, and Nagai above, teaches of a level shift circuit (Yanagi , Fig. 1, items 5a-b or Okajima, Fig. 14, item 60) connected to the one signal line directly (Yanagi , Fig. 1, item Vref1) {claim 29}; and

40. the inversion signal line directly (Okajima, Fig. 14, item 56) {claims 30-32}.

41. **In regards to claim 35,** Yanagi as modified by Okajima and Yatabe above in claims 1, 17, teaches that the at least one capacitance (Yanagi, Fig. 1, item 13) is directly connected to respective terminals of the first and second transistors (Okajima, Fig. 14, item 62, 66 and 65, 69).

42. Claims 5, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (U.S. Patent No.: 7,002,541 B2) in view of Okajima (U.S. Patent No.: 5,793,680), Yatabe et al.

(Japanese Publication No.: 2001-051662 as translated by U.S. Patent No.: 6,633,287 B1) and Park et al. (U.S. Patent No.: 7,133,034 B2).

43. **In regards to claims 5, 20,** Yanagi, Yatabke, and Okajima fails to teach that a high level voltage of each signal of the signal line is a high-level line voltage of the gate driver and

44. wherein a low-level voltage of each signal of the signal line is a low-level line voltage of the gate driver (Fig. 1).

45. Park teaches that a high level voltage of each signal of the signal line is a high-level line voltage of the gate driver and

46. wherein a low-level voltage of each signal of the signal line is a low-level line voltage of the gate driver (Fig. 1).

47. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have the high and low signal of the signal line is the high and low signal of the gate line as taught by Park with the display of Yanagi and the transistors of Okajima. This combination would allow for the gate to open so that the common voltage may be applied (Park, Fig. 1).

48. Claims 2, 6-7, 16, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (U.S. Patent No.: 7,002,541 B2) in view of Okajima (U.S. Patent No.: 5,793,680), Yatabe et al. (Japanese Publication No.: 2001-051662 as translated by U.S. Patent No.:

6,633,287 B1), Kubota et al. (U.S. Publication No.: 2002/0075249 A1) and Nagai (U.S. Patent No.: 6,011,355).

49. **In regards to claims 2, 16,** Yanagi teaches that at least the common drive circuit (Fig. 1, items 4-6), a display portion (Fig. 1, item 13) and a gate driver circuit (Fig. 1, item 2) for controlling switching of pixels of each line in the display portion (Fig. 1, item 13) are mounted on a substrate, and

50. wherein the common drive circuit (Fig. 1, items 4-5, Vcom) is disposed on a position near to the gate driver circuit (Fig. 1, item 2) and the display portion therebetween (Fig. 1, item 13).

51. Yanagi as modified by Okajima and Yatabke, fails to teach that display and driver are placed on a single substrate; and

52. that the drive circuits are disposed opposite to each other.

53. Kubota teaches that display and driver are placed on a single substrate (Fig. 76, section [0303]).

54. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have all the elements of Yanagi as modified by Okajima and Yatabke, be combined on a single substrate as taught by Kubota. This combination can reduce cost and improve reliability (Kubota, section [0303]).

55. Nagai teaches of the concept of having drive circuits are disposed opposite to each other (Fig. 1, items 2, 31).

56. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have the driver circuits of Yanagi as modified by Okajima, Yatabe, and Kubota be placed opposite to each other as taught by Nagai, since the positioning of the drivers still allows the device to perform in a similar manner (Nagai, column 3, lines 55-60).

57. **In regards to claim 6,** Yanagi as modified by Okajima, Yatabke, Kubota, and Nagai above, fails to teaches that the first and second transistors are comprised of thin-film transistors.

58. Examiner takes official notice that it is well known in the art to use thin-film transistors.

59. It would have been obvious to one with ordinary skill in the art at the time the invention was made to use thin-film transistors in the drive circuit of Yanagi as modified by Okajima, Yatabke, Kubota, and Nagai, since the use of thin-film transistors enables a simple and cost efficient method to implement a switching method.

60. **In regards to claim 7,** Yanagi teaches that the display portion comprises a liquid crystal display (Fig. 1).

61. **In regards to claim 36,** Yanagi teaches that of a common voltage generating circuit (Fig. 1, items 4-6) formed on the substrate adjacent to the common drive circuit (Fig. 1, items 4-6).

Conclusion

62. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

63. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

64. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP
10 May 2010

Tammy Pham
/Tammy Pham/
Examiner, Art Unit 2629